B.Tech (ECE) (Sem-3rd)
Analog Devices & Circuits
Subject Code: BTEC 301
Paper ID: A1130

Roll No_____

Total no of page-2

Time: 3hrs   **Maximum Marks: 60**
Instruction to Candidate:

1). Section A is compulsory consisting of Ten questions of Two marks each.
2). Section B contains Five questions carrying Five marks each and student has to attempt any Four questions.
3). Section C contains Three questions carrying Ten marks each and student has to attempt any Two questions.

Section A

Q1
  a) Give the Shockley's diode equation and label its each parameter.
  b) Give the working principle of LCD?
  c) Why FETs are classified as majority carrier devices?
  d) "Cut-off voltage is not the same thing as pinch-off voltage, although the names seem quite similar", Comment.
  e) Open loop gain of amplifier is 60000 and closed loop gain with negative feedback is 300. If there is 10% distortion without feedback, calculate distortion with feedback.
  f) Give condition for 180deg phase shift in RC phase shift oscillator.
  g) Define harmonic distortion.
  h) What are the applications of UJT?
  i) What is the difference between class A and Class AB amplifier configuration?
  j) What is stability factor?

Section B

Q2. Determine the range of R_L and I_L for the circuit shown in figure 1

$[V_Z = 10V, I_{Zm} = 32mA]$

figure: 1
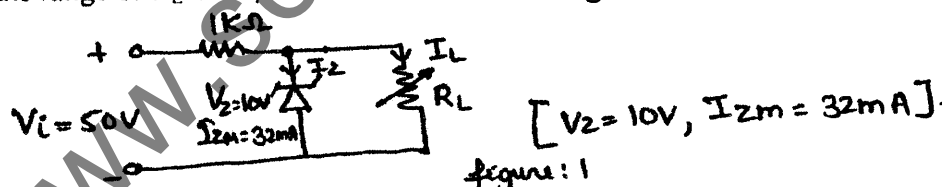
Q3. Are even harmonics present in push-pull amplifier? What is cross over distortion and how it can be removed?

Q4. Discuss the I-V Characteristics of n-channel JFET in context to the various region of operation.

Q5. Illustrate and briefly explain the principle of series voltage negative feedback. What is the effect of negative feedback on an amplifier?

Q6. Explain CB and CE junction capacitances and coupling capacitance effect at high frequencies.

Section C

Q7. Compare the performance characteristics of three BJT amplifier configurations, in qualitative terms, regarding I/O impedances and voltage and current gain.

Q8.
  a) Derive the Input and Output impedance, Current and Voltage gain of CE amplifier using h-parameter equivalent circuit.
  b) Calculate these circuit parameters for the circuit shown in figure 2. Transistor h-parameters are: $h_{fe}=75$, $h_{ie}=2.1k\Omega$, $h_{oe}=1\mu S$.
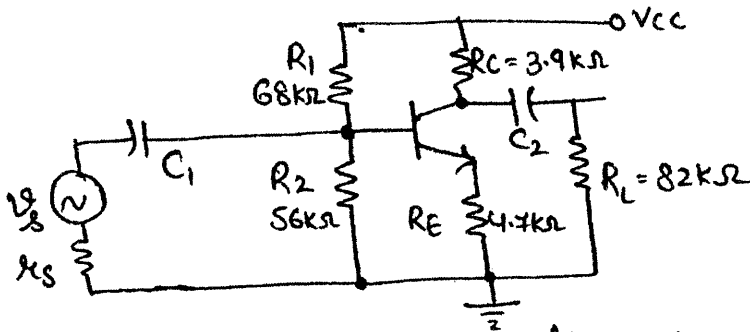

figure : 2

Q9. Design the Hartley Oscillator as shown in figure 3, that can produce a 100kHz output frequency with an amplitude of approximately $\pm$ 8V. Also calculate the minimum open loop gain. Assume $X_{L2}=1k\Omega$ and L1, L2 have no mutual inductance.
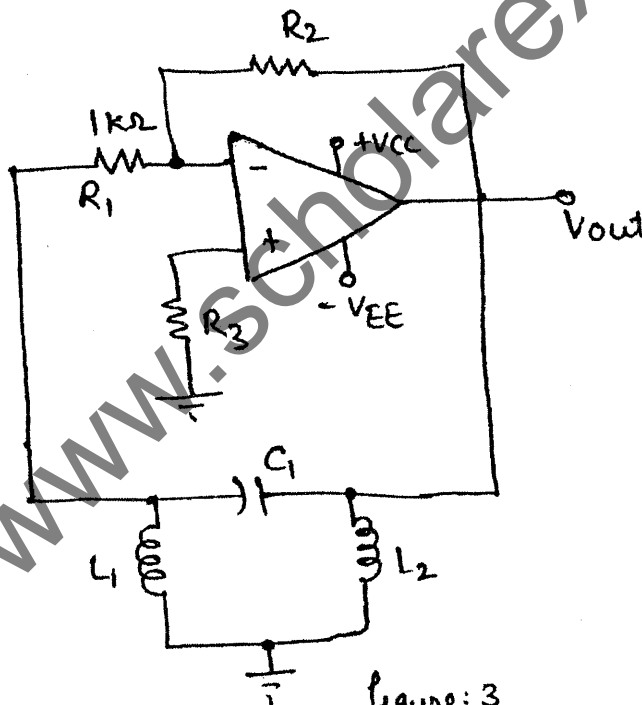

figure : 3

————End————