Roll No. | | | | | | | | | | | | |

Total No. of Pages: 02
Total No. of Questions: 09

B.Tech. (ECE/ETE) (Sem.-6th)
VLSI Design
Subject Code: BTEC-604
Paper ID: [A2318]

Time: 3 Hrs.

Max. Marks: 60

Instructions to candidates:

1) *Section-A is COMPULSORY consisting of TEN questions carrying TWO marks each.*
2) *Section-B contains FIVE questions carrying FIVE marks each. And student has to attempt any FOUR questions.*
3) *SECTION-C contains THREE questions carrying TEN marks each. And student has to attempt any TWO questions.*

SECTION-A

Q1. a) Name different types of primary constructs or design units in VHDL.

b) Name different types of operators in VHDL.

c) Write down various functions of signal drivers in VHDL?

d) Write syntax of process statement used in VHDL and in which type of modeling style it is used?

e) What parameters affect Threshold Voltage?

f) What are various sources of power dissipation in CMOS circuits?

g) What parameters of MOS transistor are scaled in constant field scaling?

h) How increase in temperature affects the performance of CMOS circuits?

i) Differentiae between a variable and signal in VHDL.

j) List various short channel effects present in MOS devices.

SECTION-B

Q2) Design a 2 × 4 decoder and write structural VHDL code.

Q3) Design a decade counter and write VHDL code.

Q4) Design XOR gate using NAND gates and write VHDL code.

Q5) Explain working of NMOS enhancement transistor and plot its output and transfer characteristics.

Q6) Explain various sources of power dissipation in CMOS circuits.

SECTION-C

Q7) Explain CMOS inverter's DC transfer characteristics and various regions of its operation. How β_n / β_p ratio influences the DC transfer characteristics?

Q8) Derive I-V equation for an enhancement type NMOS transistor and plot its output characteristics. What factors influence the current flowing between source and drain terminals?

Q9) Construct a 1-bit full adder from half-adders and logic gates. Write VHDL code.

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