Roll No.

Total No. of Pages: 02

Total No. of Questions: 09

B.Tech.(Electronics Engg.) (2012 Onwards) (Sem.-3)

B.Tech.(ECE)/(Electronics & Computer Engg.)/(ETE) (2011 Onwards)

DIGITAL CIRCUITS AND LOGIC DESIGN

Subject Code: BTEC-302 Paper ID: [A1131]

Time: 3 Hrs.

Max. Marks: 60

INSTRUCTION TO CANDIDATES:

- SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
- 2. SECTION-B contains FIVE questions carrying FIVE marks each and students has to attempt any FOUR questions.
- 3. SECTION-C contains THREE questions carrying TEN marks each and students has to attempt any TWO questions.

SECTION - A

1) Write briefly:

- (a) Explain race condition in JK flip flops. How can it be avoided?
- (b) Differentiate between PLA and ROM.
- (c) What are the advantages of ECL over other IC logic families?
- (d) Implement a full subtractor using NAND gates.
- (e) State De Morgan theorems.
- (f) How many select lines are required for 10:1 MUX?
- (g) What is the purpose of a shift register?
- (h) Define the term resolution of D/A converter.
- (i) Explain fan in, fan out, propagation delay and noise margin.
- (j) Explain the importance of binary ladder network.

SECTION - B

- 2) What is PLA? Design EX-3 to BCD code converter using PLA.
- 3) Design 3 bit MOD 6, unit distance up counter using JK flip flops.
- 4) What is a magnitude comparator? Design and draw the logic diagram of 2 bit magnitude comparator
- 5) Explain the working of R-2R ladder type DAC.
- 6) Discuss different specifications of A/D converter.

SECTION - C

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- 7) Write short notes on:
 - (a) CCD memory.
 - (b) Comparison of logic families.
- 8) (a) Explain the various design steps of asynchronous machine.
 - (b) Explain various MEV approaches to asynchronous design.
 - (c) With the help of example(s) discuss the hazards in circuits developed by MEV method.
- 9) Minimize the following using Tabular Method.

 $f(A, B, C, D, E) = \sum m(1, 3, 4, 6, 9, 11, 12, 14, 17, 19, 20, 22, 25, 27, 28, 30) + \sum d(8, 10, 24, 26).$