Roll No. | | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 09

B.Tech.(ECE)/(ETE) (2011 onwards) (Sem.–6)

VLSI DESIGN

Subject Code : BTEC-604

Paper ID : [A2318]

Time : 3 Hrs. Max. Marks : 60

INSTRUCTION TO CANDIDATES :

1. SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
2. SECTION-B contains FIVE questions carrying FIVE marks each and students has to attempt any FOUR questions.
3. SECTION-C contains THREE questions carrying TEN marks each and students has to attempt any TWO questions.

SECTION-A

1. **Write briefly :**

a) What are the design steps for a digital system? Explain by designing a half-adder.

b) How 'process' statement is significant in Behavioral Modeling of VHDL Design?

c) Using dataflow modeling in VHDL, design a 2-input AND gate.

d) Define propagation delay with reference to MOS devices.

e) Write a short note on Scaling of MOS circuits.

f) List basic components of a computer system and describe its architecture.

g) Why are Enhancement MOSFETS preferred to Depletion MOSFETS in Logic IC's?

h) List the scalar data types in VHDL taking suitable examples.

i) Explain the concept of multiple drivers for a signal.

j) Draw the CMOS inverter and discuss its characteristics.

SECTION-B

2. Illustrate the use of a package declaration and a package body with a suitable example.

3. Design a VHDL code for a 3 bit binary to gray code converter.

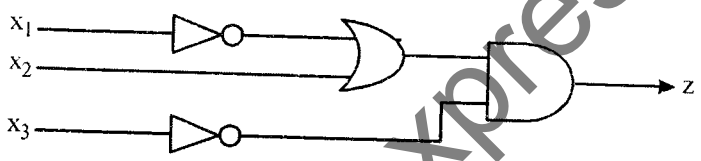
4. Write a short note on conditional statements present in VHDL for sequential modeling. Give syntax of if-else and case using suitable example.

5. For a complex/compound CMOS logic gate, how do you realize the pull the pull-up and the pull up and the pull-down networks?

6. What are the types of delays in VHDL? Explain how they can be modeled in the VHDL designs.

SECTION-C

7. Implement the given circuit using Structural style of VHDL Modeling :



8. Write VHDL description for a 3-bit binary asynchronous up counter.

9. Write points of difference among PMOS, NMOS and CMOS devices.