Roll No. $\square$

Time: 3 Hrs.
Max. Marks : 60

## INSTRUCTION TO CANDIDATES :

1. SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
2. SECTION-B contains FIVE questions carrying FIVE marks each and students has to attempt any FOUR questions.
3. SECTION-C contains THREE questions carrying TEN marks each and students has to attempt any TWO questions.

SECTION-A

1. Write briefly :
a) Define the term decoder.
b) Convert the following logic functions in a product of maxterms form.

$$
F\left(A, B, C^{\prime \prime}\right)=\left(A^{\prime}+B\right)\left(B^{\prime}+C^{\prime}\right)
$$

c) Represent ( -11 ) in 2 's compliment form using 5 bits.
d) How many select lines are required for 10 to 1 MUX?
e) Why we need shiftregisters?
f) Realize AND gate using only NOR gates.
g) Which flip flop is preferred for data transfer?
h) List various $\mathrm{A} / \mathrm{D}$ convertors.
i) Give and logic diagram and characteristics table of a clocked D flip flop.
j) What is bi-directional shift register?

## SECTION-B

2. Minimize the following equations using K Map.
a) $Y=(A+B)(A+\bar{B})(A+\bar{C})$
b) $Y=\bar{A} B+A \bar{B} C+A B$
3. Convert the following numbers :
a) $(12.25)_{10}=(?)_{2}$
b) $(10101.1101)_{2}=(?)_{8}$
c) $(125)_{8}=(?)_{10}$
d) $(34)_{16}=(?)_{2}$
e) $(67.2)_{8}=(?)_{2}$
4. What is race around condition? How it is avoided in Master Slave I lip Flop?
5. Explain how EPROM memory cell works.
6. Explain the working of carry look ahead adder.

## SECTION-C

7. Design Mode-8 synchroneus counter using T flip flops.
8. a) Write a note on three state TTL.
b) Write down merits and-demerits if TTL over MOS gates.
9. Diâw the circuit of R-2R ladder D/A converter and explain its operation. Also determine theresolution of the output from a DAC that has a 12-bit input.
